AMENDMENTS TO THE SPECIFICATION

Please replace paragraph [0018] with the following amended paragraph:

[0018] A full page of NAND Flash memory 114 may comprise a plurality of blocks of data. Thus, the NAND Flash memory controller 100 may read or write a plurality of blocks when reading or writing a full page of data. After each block of data is read or written, a typical NAND Flash memory controller 100 may calculate the ECC, transfer the ECC to the host processor 135, and then dump the ECC information. The amount of time lost in completing such processes may cause the host processor 135 to suffer a further loss in performance, especially if the transfer between the host processor and the controller is performed by a direct memory access device ("DMA"). In accordance with the preferred embodiment of the invention as described below, serialization of the ECC computation process and the addition of an automatic ECC register switching mechanism compensates for such performance losses